PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Pradeep Sindhu; Dennis C. Ferguson	Confirmation No.	4412
Serial No.:	10/004,536		
Filed:	October 31, 2001	Customer No.:	28863
Examiner:	Joseph E. Avellino		
Group Art Unit:	2143		
Docket No.:	1014-014US01/JNP-0074		
Title:	NETWORK ROUTER HAVING EMBEDDED MEMORY		

APPEAL BRIEF

Board of Patent Appeals and Interferences
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313

Dear Sir:

This is an Appeal Brief from the Final Office Action mailed June 16, 2006. The Notice of Appeal was filed on September 18, 2006. The present application has been rejected more than twice. Appellant submits this Appeal Brief in triplicate. A check for $620.00 is enclosed to cover the required fee of $500.00 for filing this Brief.

Appellant requests the opportunity for a personal appearance before the Board of Patent Appeals and Interferences to argue the issues of this appeal. The fee for the personal appearance will be timely paid upon receipt of the Examiner's Answer. Please also charge any additional fees that may be required or credit any overpayment to Deposit Account No. 50-1778.

TABLE OF CONTENTS

	Page
Real Party in Interest	3
Related Appeals and Interferences	3
Status of Claims	3
Status of Amendments	3
Summary of the Claimed Subject Matter	4
Grounds of Rejection to be Reviewed on Appeal	11
Arguments of Appellant	12
Appendix: Claims on Appeal	20
Appendix: Evidence	27
Appendix: Related Proceedings	28

REAL PARTY IN INTEREST

The real party in interest is Juniper Networks, Inc. of Sunnyvale, California.

RELATED APPEALS AND INTERFERENCES

There are no related appeals and interferences.

STATUS OF CLAIMS

Claims 1-9, 11-20, 22-26, 28-32 and 34-35 are on appeal in this case. All claims are rejected under 35 U.S.C. 103(a) as being unpatentable over Mathur (USPN 6,424,658) in view of Muller et al. (USPN 6,245,680). All claims are being appealed.

STATUS OF AMENDMENTS

No amendments have been filed subsequent to the Final Office Action mailed June 16, 2006 from which this Appeal has been made.

SUMMARY OF THE CLAIMED SUBJECT MATTER

A concise summary of independent claim 1, 9, 18, 24, 30 and 35 is provided below with reference to the specification and figures.

Independent claim 1

Claim 1 is directed to *a routing component of a router*. FIG. 1 shows a router 10 having one or more routing components 12A and 12B. FIG. 2 shows routing component 12A in more detail.

Claim 1 requires that the routing component include *a first interface to communicate data with a network; and a second interface to communicate data to a second routing component using a switch internal to the router.* FIG. 2 shows routing component 12A having a first interface (interface modules 20) to communicate data to a network and a second interface (interface modules 20) to communicate data to a second routing component (routing component 12A of FIG. 1) using a switch internal to the router (switch fabric 16).

Claim 1 requires that *the first interface and the second interface are integrated within a single integrated circuit.* Routing component 12A, including interface modules 20, is described as implemented within an ASIC or other integrated circuit (IC) on pg. 6, ll. 19-21.

Claim 1 requires that *the routing component include an embedded memory within the integrated circuit*, and *a memory interface to couple the integrated circuit to an external memory.* FIG. 2 shows embedded memory 34 within routing component 12A, and a memory interface 32 to memory 30 that is external to routing component 12A.

Claim 1 requires *at least one control unit that receives data from the network via the first interface and accesses a forwarding table to determine a network destination for the data.* FIG. 2 shows at least one control unit (control units 26A and 26B) that receive data from the network via the first interface (WAN interface 14 and interface modules 20). FIG. 2 also shows the control unit as coupled to forwarding tables 28. At pg. 6, ln. 28 – pg. 7, ln. 4 and pg. 9, ll. 2-4, the at least one control unit (control units 26A and 26B) is described as receiving an inbound packet from the network and forwarding the inbound

packet to outbound link 6 or another routing component based on information stored in the forwarding tables 28.[1]

Claim 1 requires that the control unit *buffer the data using the embedded memory internal to the integrated circuit when the destination requires forwarding the data to the second routing component of the router using the switch.* Pg. 7, ll. 19-32 describes control unit 26A buffering the data from the network within small, high-speed embedded memory 34 within the integrated circuit when the control unit determines that the network data is destined for a second routing component because switch fabric 16 has a high bandwidth and the data is less likely to experience congestion.

Claim 1 also requires that the control unit *buffers the data in the external memory when the destination requires forwarding the data to the network via the first interface.* Pg. 7, ll. 5-18, describes control unit 26B buffering the data from the network within a large, external memory device 30 when the control unit determines that the data is destined for the network because WAN interface 14 typically has a low bandwidth and the packets are more likely to experience congestion.

Independent claim 9

Claim 9 is directed to a *network element comprising a first network interface to communicate data with a network, a second network interface to communicate data with the network.* FIG. 1 shows a network element (router 10) having a first network interface (WAN interface 14A) and a second network interface (WAN 14B).

Claim 9 requires that the network element include *a routing component formed in an integrated circuit, wherein the routing component has an embedded memory within the integrated circuit.* Claim 9 also requires *a second memory external to the routing component.* FIG. 2 and pg. 6, ll. 19-21 describe a routing component 12A as an ASIC or other integrated circuit (IC). FIG. 2 shows embedded memory 34 within routing component 12A and memory 32 that is external to the routing component.

Claim 9 requires that routing component *receives data from the first network interface and accesses a forwarding table to determine a network destination for the*

---

[1] See also, pg. 1, ll. 20-27 (describing the use of forwarding information to determine network destinations for purposes of forwarding packets).

data. FIG. 2 shows control units 26A and 26B coupled to forwarding tables 28. At pg. 6, ln. 28 – pg. 7, ln. 4, control units 26A and 26B are described as storing forwarding tables 28 and, upon receiving an inbound packet, forwarding the inbound packet to outbound link 6 or another routing component via switch fabric 16. Pg. 1, ll. 20-27 describes routers using forwarding information to determine network destinations for purposes of forwarding packets.

Claim 9 requires that *the routing component buffer data in the embedded memory internal to the routing component when the destination requires forwarding the data to a second routing component using a switch internal to the network element.* Pg. 7, ll. 19-32 describes control unit 26A buffering network data within small, high-speed embedded memory 34 within the integrated circuit when the control unit determines that the network data is destined for a second routing component because switch fabric 16 has a high bandwidth and the data is less likely to experience congestion.

Claim 9 requires that the routing component *buffer data communicated in the second memory external to the routing component when the destination requires forwarding the data to the network via the first network interface.* Pg. 7, ll. 5-18, describes control unit 26B buffering data within a large, external memory device 30 when the control unit determines that the data is destined for the network because WAN interface 14 typically has a low bandwidth and the packets are more likely to experience congestion.

Independent claim 18

Independent claim 18 is directed to an *integrated circuit* comprising *a first interface to communicate data with a network at a first data rate,* and *a second interface to communicate data with a switch fabric at a second data rate higher than the first data rate.* As summarized above, FIG. 2 and pg. 6, ln. 19 - pg. 8, ln. 2 describe an integrated circuit (routing component 12A) having interface modules 20 to communicate data to WAN interface 14 at low bandwidth and to switch fabric 16 having a high bandwidth.

Claim 18 further requires *an embedded memory internal to the IC*, and *an interface to a memory external to the IC.* FIG. 2 shows embedded memory 34 within

routing component 12A, and a memory interface 32 to memory 30 that is external to routing component 12A.

Claim 18 requires *at least one control unit that receives data from the first interface and accesses a forwarding table to determine a network destination for the data.* At pg. 6, ln. 28 – pg. 7, ln. 4 and pg. 9, ll. 2-4, control units 26A and 26B are described as receiving an inbound packet and forwarding the inbound packet to either outbound link 6 or another routing component via switch fabric 16 based on information stored in the forwarding tables 28. Pg. 1, ll. 20-27 describes using forwarding information to determine network destinations for purposes of forwarding packets.

Claim 18 further requires that the control unit *buffer data in the embedded memory internal to the integrated circuit when the destination requires forwarding the data using the switch fabric,* and that the control unit *buffer the data using the external memory when the destination requires forwarding the data out to the network via the first interface.* As summarized above with respect to claim 1, pg. 7, ll. 19-32 describes control unit 26A buffering network data within small, high-speed embedded memory 34 within the integrated circuit when the control unit determines that the network data is destined for a second routing component because switch fabric 16 has a high bandwidth and the data is less likely to experience congestion. Conversely, pg. 7, ll. 5-18, describes control unit 26B buffering data within a large, external memory device 30 when the control unit determines that the data is destined for the network because WAN interface 14 typically has a low bandwidth and the packets are more likely to experience congestion.

Independent claim 24

Claim 24 is directed to a *router* comprising *an integrated circuit (IC)* having *a first interface to communicate data with a network, a second interface to communicate data with a switch fabric internal to the router, an embedded memory, an interface to a memory external to the IC, and at least one control unit that receives data from the network via the first interface and accesses a forwarding table to determine a network destination for the data.* As summarized above, FIG. 1 shows a router 10. FIG. 2 and pg. 6, ln. 19 - pg. 8, ln. 2 describe an integrated circuit (routing component 12A) having interface modules 20 to communicate data to a network via WAN interface 14 and to

switch fabric 16 internal to router 10. FIG. 2 shows the integrated circuit (routing component 12A) having an internal embedded memory 34 and a memory interface 32 to memory 30 that is external to the integrated circuit. FIG. 2 shows control units 26A and 26B coupled to forwarding tables 28. At pg. 6, ln. 28 – pg. 7, ln. 4 and pg. 9, ll. 2-4, control units 26A and 26B are described as receiving an inbound packet and forwarding the inbound packet to either outbound link 6 or another routing component via switch fabric 16 based on information stored in the forwarding tables 28. Pg. 1, ll. 20-27 describes using forwarding information to determine network destinations for purposes of forwarding packets.

Claim 24 requires that the control unit *buffer the data using the embedded memory internal to the integrated circuit when the destination requires forwarding the data to a routing component of the router using the switch fabric.* Pg. 7, ll. 19-32 describes control unit 26A buffering network data within small, high-speed embedded memory 34 within the integrated circuit when the control unit determines that the network data is destined for a second routing component because switch fabric 16 has a high bandwidth and the data is less likely to experience congestion.

Claim 24 requires that the control unit *buffer the data in the external memory when the destination requires forwarding the data to the network via the first interface.* Pg. 7, ll. 5-18, describes control unit 26B buffering data within the large, external memory device 30 when the control unit determines that the data is destined for the network because WAN interface 14 typically has a low bandwidth and the packets are more likely to experience congestion.

Independent claim 30

Claim 30 recites a method for communicating data using a network router. Claim 30 requires *receiving inbound data from a network interface via a first routing component*, and *accessing a forwarding table with a control unit of the network router to determine a network destination for the data.* FIG. 3 and pg. 8, ln. 28- pg. 9, ln. 17 shows receiving an inbound packet (block 40) and using information within forwarding tables to forward the packet (blocks 44, 46).

Claim 30 requires *when the destination requires forwarding the data to a second routing component internal to the router using a switch having a higher bandwidth than the network interface, buffering the inbound data within an embedded memory internal to the first routing component.* Pg. 7, ll. 19-32 describes control unit 26A buffering network data within small, high-speed embedded memory 34 within the integrated circuit when the control unit determines that the network data is destined for a second routing component because switch fabric 16 has a high bandwidth and the data is less likely to experience congestion.

Claim 30 requires *forwarding the inbound data from the first routing component to a second routing component via the switch.* FIG. 3 (block 46) and pg. 9, ll. 11-17 describes forwarding an inbound packet from WAN interface 14 to a second routing component switch fabric 16.

Claim 30 requires *receiving outbound data with the first routing component from the switch and, when the destination requires forwarding the outbound data to the network interface having a lower bandwidth than the switch, buffering the outbound data within a memory external to the first routing component.* Pg. 7, ll. 5-18, describes control unit 26B buffering data within a large, external memory device 30 when the control unit determines that the data is destined for the network because WAN interface 14 typically has a low bandwidth and the packets are more likely to experience congestion.

Claim 30 requires *forwarding the outbound data to the network interface.* FIG. 3 (block 46) and pg. 9, ll. 6-11 describes forwarding a packet from switch fabric 16 to WAN interface 14.

Independent claim 35

Claim 35 is directed to a *routing arrangement* comprising *a crossbar arrangement* and *a plurality of routing components coupled to the crossbar arrangement.* FIG. 1 shows a routing arrangement (router 10) having a crossbar arrangement (switch fabric 16) and a plurality of routing components (routing components 12A, 21B).

Claim 35 requires that *at least a first one of the routing components comprise a first interface to communicate data with a network, a second interface to communicate data with the crossbar arrangement, an embedded memory, an external memory interface*

to a memory external to the routing component, and at least one control unit that receives data from the first interface and determines a network destination for the data. As summarized above, FIG. 2 and pg. 6, ln. 19 - pg. 8, ln. 2 describe a routing component 12A having a first interface (interface modules 20) to communicate data to a network and a second interface (interface modules 20) to communicate data to a crossbar arrangement (switch fabric 16). FIG. 2 shows the routing component 12A having an internal embedded memory 34 and a memory interface 32 to memory 30 that is external to the integrated circuit. FIG. 2 shows control units 26A and 26B coupled to forwarding tables 28. At pg. 6, ln. 28 – pg. 7, ln. 4 and pg. 9, ll. 2-4, control units 26A and 26B are described as receiving data from the network and forwarding the data based on information stored in the forwarding tables 28.

Claim 35 requires that the control unit *buffer the data using the embedded memory internal to the routing component when the destination requires forwarding the data to a second one of the routing components using the crossbar arrangement.* Pg. 7, ll. 19-32 describes control unit 26A buffering network data within small, high-speed embedded memory 34 within the integrated circuit when the control unit determines that the network data is destined for a second routing component because switch fabric 16 has a high bandwidth and the data is less likely to experience congestion.

Claim 35 requires that the control unit *buffer the data in the external memory when the destination requires forwarding the data to the network via the first interface.* Pg. 7, ll. 5-18, describes control unit 26B buffering data within a large, external memory device 30 when the control unit determines that the data is destined for the network because WAN interface 14 typically has a low bandwidth and the packets are more likely to experience congestion.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The only grounds for rejection to be reviewed on Appeal is the rejection of claims 1-9, 11-20, 22-26, 28-32 and 34-35 under 35 U.S.C. 103(a) as being unpatentable over Mathur (USPN 6,424,658) in view of Muller et al. (USPN 6,245,680).

ARGUMENTS

<u>The First Ground of Rejection</u>

Claims 1-9, 11-20, 22-26, 28-32 and 34-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mathur (USPN 6,424,658) in view of Muller et al. (USPN 6,245,680).

With respect to the first ground of rejection, Appellant argues claims 1-9, 11-20, 22-26, 28-32 and 34-35 as a group, as set forth below. Appellant directs the Board to independent claim 1.

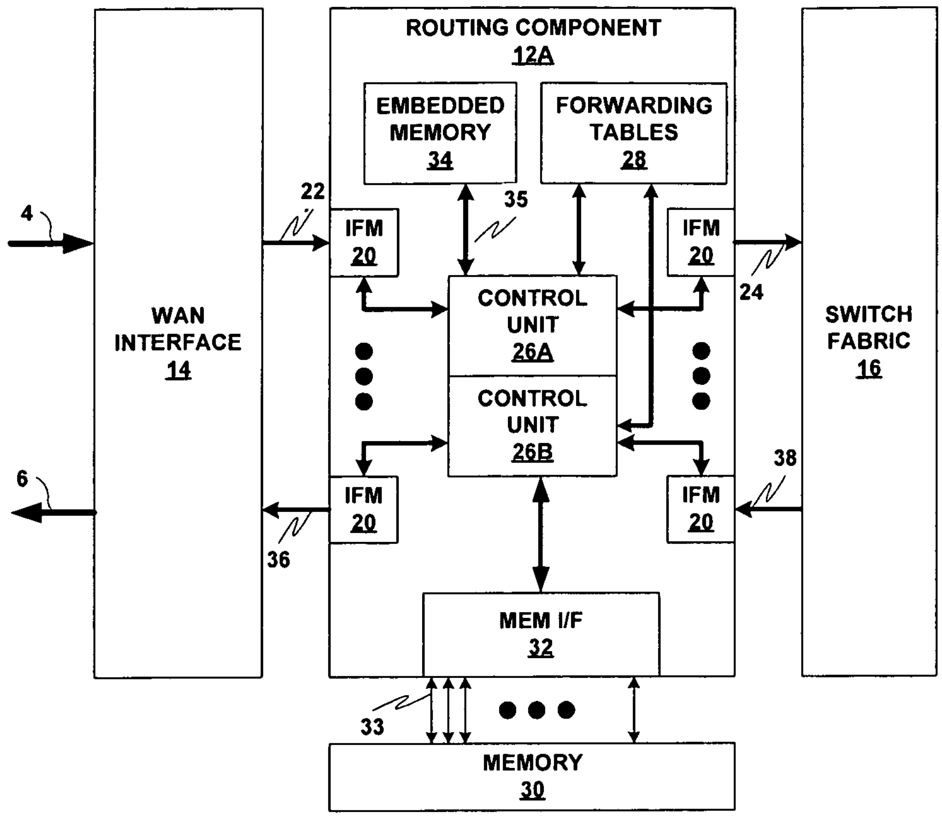
Claim 1

As discussed above, claim 1 is directed to a routing component within a router, the routing component comprising a first interface to communicate data with a network and a second interface to communicate data to a second routing component using a switch internal to the router. Claim 1 requires that the first interface and the second interface are integrated within a single integrated circuit. Claim 1 also requires that the routing component include an embedded memory within the integrated circuit, and a memory interface to couple the integrated circuit to an external memory.

Claim 1 further recites at least one control unit that receives data from the network via the first interface and accesses a forwarding table to determine a network destination for the data. Claim 1 requires that the control unit buffer the data using the embedded memory internal to the integrated circuit when the destination requires forwarding the data to the second routing component of the router using the switch. In addition, claim 1 requires that the control unit buffer the data in the external memory when the destination requires forwarding the data to the network via the first interface.

In this manner, the literal language of claim 1 is directed to a routing component in which data received from the network on the <u>same</u> interface (e.g., inbound packets from WAN interface 14) are buffered differently by using either embedded memory or external memory based on the particular destination to which the data is to be forwarded.

To illustrate this by way of example in reference to the present application, Appellant directs the Board to FIG. 2, reproduced below:



With respect to FIG. 2, the present application states that upon receiving an inbound packet via input link 4, control units 26A, 26B of routing component 12A may forward that inbound packet either directly to outbound link 6 via WAN interface 14 or to another routing component via internal switch fabric 16.[2] In this manner, in the described embodiment, a data packet received on the same interface (e.g., an inbound packet received from the network via link 4) may be forwarded directly back to the network as an outbound packet using a network interface of the same bandwidth (e.g., WAN interface 14) or forwarded to another routing component by the internal switch fabric 16 having a different bandwidth. In this regard, when forwarding packets, control units 26 of routing component 12A actively make buffering decisions based on the destination for the particular data (e.g., packet). That is, as described at length in the application, data

[2] Pg. 6, ln. 26-pg. 7, ln. 5.

received from an interface, such as inbound packets received from the network, is buffered differently (i.e. using either embedded memory 34 or external memory 30) based on the destination specified within the packet and the bandwidth differences between the interfaces.

For example, pg. 7, ll. 19-32 describes buffering network data within small, high-speed embedded memory 34 within the integrated circuit when it is determined that the network data is destined for a second routing component within the router because switch fabric 16 has a high bandwidth and the data is less likely to experience congestion. Conversely, pg. 7, ll. 5-18, describes buffering data within a large, external memory device 30 when it is determined that the data is destined for the network because WAN interface 14 typically has a low bandwidth and the packets are more likely to experience congestion.

This feature of selecting between internal (i.e., on-chip) and external (i.e., off-chip) memory to buffer data based on a destination to which the data is to be forwarded is a requirement of claim 1. Claim 1 specifically requires that the at least one control unit buffer the data received from the network using the embedded memory internal to the integrated circuit when the destination requires forwarding the data to the second routing component of the router using the switch, and buffer the data from the network in the external memory when the destination requires forwarding the data to the network via the first interface. In this manner, the literal language of claim 1 is directed to a routing component in which data (e.g., inbound packets) received from the network on the same interface is buffered differently, i.e. using either internal or external memory, based on the particular destination to which the packet is to be forwarded.

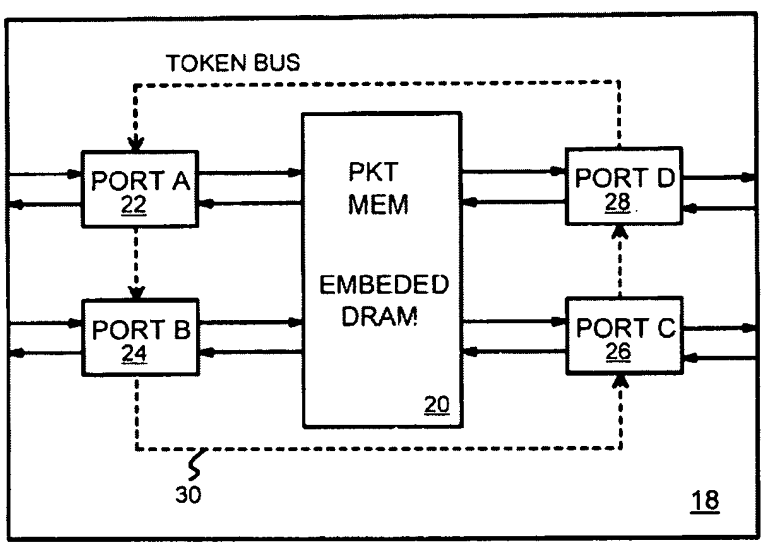
In the Final Office Action, the Examiner argued that Mathur discloses a routing component having substantially all of the features of Applicant's independent claims, but acknowledged that Mathur utilizes only internal memory and does not disclose use of an external memory. With respect to these features, the Examiner cited Muller as disclosing a routing element that utilizes external memory. Based on the Mathur reference that describes using entirely internal memory and the Muller reference that describes using entirely external memory, the Examiner concluded that it would have been obvious to one

of ordinary skill to modify the Mathur routing component in view of Muller to achieve Applicant's claimed invention.[3]

Mathur in view of Muller fails to teach or suggest a routing component having a control unit that buffers the data received from the network using the embedded memory internal to the integrated circuit when the destination requires forwarding the data to the second routing component of the router using the switch, and buffers the data from the network in the external memory when the destination requires forwarding the data to the network via the first interface. For these or similar reasons, Mathur in view of Muller fails to teach or suggest the elements of independent claims 9, 18, 24, 30 and 35.

Mathur (USPN 6,424,658)

Mathur describes a store-and-forward network switch that uses an embedded dynamic-random-access memory (DRAM) packet memory. In particular, FIG. 2 of Mathur shows a network switch chip 18 that receives packets from one of four ports A, B, C, D and stores the packets in embedded DRAM packet memory 20. The network switch chip 18 transmits the stored packets out to one or more of the four ports A, B, C, D. The following is a reproduction of FIG. 2 of Mathur:



[3] See Office Action pg. 3.

As shown in FIG. 4, Mathur makes clear that <u>all</u> packets forwarded between ports 22-28 are stored in embedded packet memory 20. For example, at col. 6, ll. 3-7, Mathur specifically states the following:

> *Port logic 22, 24, 26, 28 are bi-directional ports to a network node connected to a computer, peripheral, LAN segment, or other network equipment such as another switch, router, repeater, bridge or hub. Packets may be input or output from any port. When a packet is received by port logic 22, 24, 26, 28, it first writes the packet into embedded DRAM packet memory 20.*

Thus, as stated above and illustrated in FIG. 2 (above), Mathur teaches a switch in which packets forwarded between any of the four interface ports 22-26 are buffered within an embedded packet memory 20 regardless of the forwarding operation. With respect to buffering packets, no regard is given to the destination of the packet. In fact, no decision is made whatsoever, let alone with respect to which type of memory to use to buffer the packet. All packets forwarded between ports 22-28 are stored in embedded packet memory 20 regardless of destination or any other criteria. No controller determines destinations for packets received from the same interface and then buffers the packets differently based on the respective destinations.

Muller et al. (USPN 6,246,680)

Muller describes a highly integrated multi-layer switch element. According to Muller, the switch element includes multiple ports for transmitting and receiving packets over a network. FIG. 2 of Muller illustrates the described switch element:

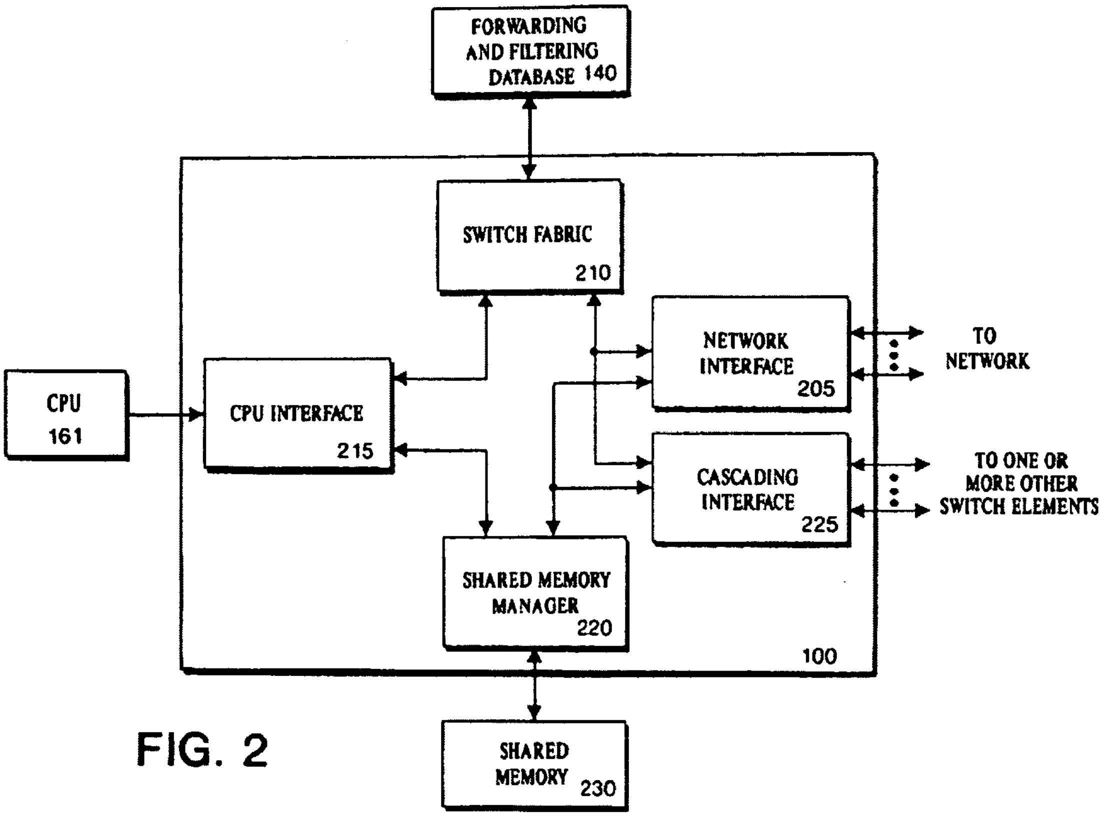


FIG. 2

Like Mathur, no regard is given to the destination specified within a packet when buffering the packet. The only relevant difference between the two references is that, unlike Mathur, Muller makes use entirely of external memory, i.e., external shared memory 230, to buffer all packets flowing between any of the network interfaces 205. For example, col. 1, ll. 41-60 of Muller states:

> *Input packet processing includes the following: (1) receiving and verifying incoming Ethernet packets, (2) modifying packet headers when appropriate, (3) requesting buffer pointers from the shared memory manager 220 for storage of incoming packets, (4) requesting forwarding decisions from the switch fabric block 210, (5)* ***transferring the incoming packet data to the shared memory manager 220 for temporary storage in an external shared memory 230****, and (5) upon receipt of a forwarding decision, forwarding the buffer pointer(s) to the output port(s) indicated by the forwarding decision. Output packet processing*

> *may be performed by one or more output ports of the network interface 205. Output processing includes* ***requesting packet data from the shared memory manager 220****, transmitting packets onto the network, and requesting deallocation of buffer(s) after packets have been transmitted. (emphasis added).*

Thus, Muller teaches a switch in which an external shared memory 230 is used to buffer all packets flowing in between network interfaces 205. No controller determines destinations of packets received from the same interface and then buffers the packets differently based on the respective destinations.

As a result, Mathur in view of Muller fails to teach or suggest a routing component in which data (e.g., packets) received on the same interface may be buffered differently, i.e. using either internal or external memory, based on the particular destination of the packet. For these reasons, neither Mathur nor Muller, either singularly or in combination, teach or suggest a routing component having a controller that buffers data received from a network via a first interface using the embedded memory internal to the routing component when a destination of the data requires forwarding the data to a second one of the routing components using the crossbar arrangement, and buffers the data received from the network via the first interface in the external memory when the destination requires forwarding the data to the network, as required by amended claim 1.

Moreover, the combination of references fails to even teach or suggest a routing component that utilizes two different types of memory (embedded memory and external, off-chip memory), for buffering of packets. As described above, Mathur specifically teaches the use of an embedded memory for buffering <u>all</u> data. Similarly, Muller teaches use of a shared memory for buffering <u>all</u> data. Modification of Mathur in view of Muller would result in use of a different memory type (i.e., external memory) to buffer packets in Mathur, but nevertheless use of external memory for all packets. Thus, neither Mathur nor Muller, either singularly or in combination, provide a suggestion of a routing component that utilizes two different types of memories, and a controller that buffers data from the same interface differently depending upon the destination of the packets in accordance with a forwarding table, as required by claim 1.

Conclusion of Arguments

The Examiner erred in rejecting Appellant's claims under 35 U.S.C. 103(a) as being unpatentable over Mathur (USPN 6,424,658) in view of Muller et al. (USPN 6,245,680). Reversal of this rejection and allowance of the pending claims are requested.

Respectfully submitted,

Date: December 11, 2006

By:

Kent J. Sieffert

Name: Kent J. Sieffert
Reg. No.: 41,312

Shumaker & Sieffert, P.A.
8425 Seasons Parkway, Suite 105
St. Paul, Minnesota 55125
Telephone: (651) 735-1100 ext. 11
Facsimile: (651) 735-1102

APPENDIX: CLAIMS ON APPEAL

Claim 1 (Previously Presented): A routing component of a router comprising:

a first interface to communicate data with a network;

a second interface to communicate data to a second routing component using a switch internal to the router, wherein the first interface and the second interface are integrated within a single integrated circuit;

an embedded memory within the integrated circuit;

a memory interface to couple the integrated circuit to an external memory; and

at least one control unit that receives data from the network via the first interface and accesses a forwarding table to determine a network destination for the data;

wherein the control unit buffers the data using the embedded memory internal to the integrated circuit when the destination requires forwarding the data to the second routing component of the router using the switch, and

wherein the control unit buffers the data in the external memory when the destination requires forwarding the data to the network via the first interface.

Claim 2 (Previously Presented): The routing component of claim 1, wherein the at least one control unit comprises:

a first control unit to buffer in the embedded memory data that is received from the first interface and forwarded to the second interface; and

a second control unit to buffer in the external memory data that is received from the second interface and forwarded to the first interface.

Claim 3 (Original): The routing component of claim 2, wherein the external memory has a greater storage capacity than the embedded memory.

Claim 4 (Original): The routing component of claim 1, wherein the first interface comprises a wide area network (WAN) interface.

Claim 5 (Original): The routing component of claim 1, wherein the second interface comprises a switch fabric interface.

Claim 6 (Original): The routing component of claim 5, wherein the switch fabric interface communicates crossbar data.

Claim 7 (Previously Presented): The routing component of claim 1, wherein the routing component is implemented using a single application specific integrated circuit (ASIC).

Claim 8 (Original): The routing component of claim 1, wherein the embedded memory comprises a random access memory (RAM).

Claim 9 (Previously Presented): A network element comprising:

a first network interface to communicate data with a network;

a second network interface to communicate data with the network;

a routing component formed in an integrated circuit, wherein the routing component has an embedded memory within the integrated circuit; and

a second memory external to the routing component,

wherein the routing component receives data from the first network interface and accesses a forwarding table to determine a network destination for the data,

wherein the routing component buffers data in the embedded memory internal to the routing component when the destination requires forwarding the data to a second routing component using a switch internal to the network element, and

wherein the routing component buffers data communicated in the second memory external to the routing component when the destination requires forwarding the data to the network via the first network interface.

Claim 10 (Cancelled).

Claim 11 (Previously Presented): The network element of claim 9, wherein the second memory has a greater storage capacity than the embedded memory.

Claim 12 (Previously Presented): The network element of claim 9, wherein the first network interface and the second network interface comprise wide area network (WAN) interfaces.

Claim 13 (Previously Presented): The network element of claim 9, further comprising a crossbar switch fabric coupling the routing component to a second routing component.

Claim 14 (Previously Presented): The network element of claim 13, wherein the switch fabric communicates crossbar data.

Claim 15 (Previously Presented): The network element of claim 9, wherein the routing component is implemented using an application specific integrated circuit (ASIC).

Claim 16 (Original): The network element of claim 9, wherein the embedded memory comprises a random access memory (RAM).

Claim 17 (Previously Presented): The network element of claim 9, wherein the second routing component includes an embedded memory to store data communicated using the second network interface.

Claim 18 (Previously Presented): An integrated circuit (IC) comprising:

a first interface to communicate data with a network at a first data rate;

a second interface to communicate data with a switch fabric at a second data rate higher than the first data rate;

an embedded memory internal to the IC;

an interface to a memory external to the IC; and

at least one control unit that receives data from the first interface and accesses a forwarding table to determine a network destination for the data,

wherein the control unit buffers data in the embedded memory internal to the integrated circuit when the destination requires forwarding the data using the switch fabric, and

wherein the control unit buffers the data using the external memory when the destination requires forwarding the data out to the network via the first interface.

Claim 19 (Original): The IC of claim 18, wherein the memory external to the IC has a greater storage capacity than the embedded memory.

Claim 20 (Original): The IC of claim 18, wherein the first interface is coupled to a wide area network (WAN) interface.

Claim 21 (Cancelled).

Claim 22 (Previously Presented): The IC of claim 18, wherein the switch fabric comprises a crossbar.

Claim 23 (Original): The IC of claim 18, wherein the embedded memory comprises a random access memory (RAM).

Claim 24 (Previously Presented): A router comprising:

an integrated circuit (IC) comprising:

a first interface to communicate data with a network;

a second interface to communicate data with a switch fabric internal to the router;

an embedded memory; and

an interface to a memory external to the IC; and

at least one control unit that receives data from the network via the first interface and accesses a forwarding table to determine a network destination for the data,

wherein the control unit buffers the data using the embedded memory internal to the integrated circuit when the destination requires forwarding the data to a routing component of the router using the switch fabric, and

wherein the control unit buffers the data in the external memory when the destination requires forwarding the data to the network via the first interface.

Claim 25 (Original): The router of claim 24, wherein the memory external to the IC has a greater storage capacity than the embedded memory.

Claim 26 (Original): The router of claim 24, wherein the first interface is coupled to a wide area network (WAN) interface.

Claim 27 (Cancelled).

Claim 28 (Previously Presented): The router of claim 24, wherein the switch fabric comprises a crossbar.

Claim 29 (Original): The router of claim 24, wherein the embedded memory comprises a random access memory (RAM).

Claim 30 (Previously Presented): A method for communicating data using a network router, the method comprising:

receiving inbound data from a network interface via a first routing component;

accessing a forwarding table with a control unit of the network router to determine a network destination for the data;

when the destination requires forwarding the data to a second routing component internal to the router using a switch having a higher bandwidth than the network interface, buffering the inbound data within an embedded memory internal to the first routing component;

forwarding the inbound data from the first routing component to a second routing component via the switch;

receiving outbound data with the first routing component from the switch;

when the destination requires forwarding the outbound data to the network interface having a lower bandwidth than the switch, buffering the outbound data within a memory external to the first routing component; and

forwarding the outbound data to the network interface.

Claim 31 (Previously Presented): The method of claim 30, wherein the external memory has a greater storage capacity than the embedded memory.

Claim 32 (Previously Presented): The method of claim 30, wherein the first network interface comprises a wide area network (WAN) interface.

Claim 33 (Canceled).

Claim 34 (Previously Presented): The method of claim 30, wherein the switch communicates crossbar data.

Claim 35 (Previously Presented): A routing arrangement comprising:

a crossbar arrangement;

a plurality of routing components coupled to the crossbar arrangement, at least a first one of the routing components comprising:

a first interface to communicate data with a network;

a second interface to communicate data with the crossbar arrangement;

an embedded memory;

an external memory interface to a memory external to the routing component ; and

at least one control unit that receives data from the first interface and determines a network destination for the data,

wherein the control unit buffers the data using the embedded memory internal to the routing component when the destination requires forwarding the data to a second one of the routing components using the crossbar arrangement, and

wherein the control unit buffers the data in the external memory when the destination requires forwarding the data to the network via the first interface.

APPENDIX: EVIDENCE

None

APPENDIX: RELATED PROCEEDINGS

None